● Dr. You Zhiqiang

<Profile>

Nationality: China

Educational Background in Japan:

April 2003 – March 2006

Graduate school of Information Science, Nara Institute of Science and Technology (Doctor)

Major Field: VLSI testing

Present Institution / Status: Hunan University / Teacher

(Image) Dr. You Zhiqiang

<Follow-up Research Fellowship>

Period: June 1, 2009 – August 29, 2009 (90 days)

Host University: Nara Institute of Science and Technology

Research Topic: A low power test pattern generation methodology for VLSI based on scan chain disabling technique

Outline of research

Scan chain disabling technique efficiently reduces test power. This work would propose a test pattern generation method for the circuits this technique. The proposed technique/method should achieve short test application time and low test power especially low peak power compared with those of conventional full scan design. This research also focuses on the extended compatibility scan tree technique which reduces test application time and test power for given test set effectively. However, the test pin or/and hardware overheads are so high. A response compactor for this technique needs to be proposed to reduce the overheads.

Results of research

We proposed a low peak power test scheme and a short test application time test pattern generation scheme for the circuits using scan chain disabling technique. We also proposed a test generation method based on the schemes. In the proposed method, we use the information of scan chain disabling when performing test generation. Using the CAD tools at the host institute, the efficiency of the proposed method is proved. We plan to submit this work to DATE2010. Furthermore, we proposed a response compactor for extended compatibility scan tree construction. This work is accepted and will be published in the proceedings of IEEE 8th International Conference on ASIC in Oct. 2009.

Further research plan

We will do the experiments for our previous method in the same condition with the proposed one to evaluate the efficiency of our proposed method. After that, this complete work will be submitted to a journal. In our future work, we will try to reduce test generation time and test application time more by developing a new test generation tool, doing more effective compaction for the proposed schemes and reconstructing the sub-scan chains. Our future work will investigate also into the feasibility of these schemes to other fault models.

● Research Advisor: Professor FUJIWARA Hideo

①研究課題 / Theme of Research

A low power test pattern generation methodology for VLSI based on scan chain disabling technique

②研究概要 / Outline of Research

スキャンチェーン無効化技術は、低消費電力ＶＬＳＩテストに有効である。本研究では、スキャンチェーン無効化技術向けのテストパターン生成法を提案することで、低消費電力でかつテスト実行時間の短いテストシステムを提案する。また、与えられたテストパターン集合に対し、テスト実行時間とテスト時の消費電力を削減するための手法であるスキャンツリー構造に対する応答圧縮器を提案し、ハードウェアオーバヘッドを削減する。

③研究成果 / Results of Research

スキャンチェーン無効化技術のためのテストパターン生成を提案した。提案法では、スキャンチェーン無効化情報をテスト生成時に考慮することで、テスト実行時間の短縮に成功した。さらに、提案法を受入大学の既設の実験ツールを用いて評価実験を行い有効性を示した。また、スキャンツリー構造に対する応答圧縮器を提案し、IEEE 8th International Conference on ASICに採択され、2009年10月に発表する。

④今後の計画 / Further Research Plan

今後は、スキャンチェーン無効化技術のためのテストパターン生成法での提案法の評価と同じ条件で従来法の評価を行い、結果を国際会議や論文誌に投稿する。また、提案法をさらに改良し、テスト実行時間だけでなくテスト生成時間の短縮を行う。

研究打ち合わせ（井上准教授と）

研究成果発表（コンピュータ設計学講座にて）